

REMARKS

Claims 1-10, 13, 16, 18-28, 31, 34, 36-43, 45, 48, and 50-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsu, *et al.* (U.S. Patent Number 6,461,955) in view of Aoi (U.S. Patent Number 6,387,824) and Lee, *et al.* (U.S. Patent Number 6,171,951). Claims 17, 35 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsu, *et al.* in view of Aoi, and Lee, *et al.* and further in view of Robinson, *et al.* (U.S. Patent Number 4,201,579). Claims 11-12, 14-15, 29-30, 32-33, 44 and 46-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsu, *et al.* in view of Aoi and Lee, *et al.*, and further in view of Lui (U.S. Patent Number 6,391,761). In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention of claims 1-20, a method of fabricating dual damascene interconnections includes forming a hybrid dielectric layer on a substrate, and forming a via in the dielectric layer. The via formed in the dielectric layer is filled with a carbon-free inorganic filler. The method further includes processing the surface of the carbon-free inorganic filler filling the via formed in the dielectric layer using plasma.

In the present invention of claims 21-38, a method of fabricating dual damascene interconnections includes forming an organo silicate glass layer on a substrate, and forming a via in the organo silicate glass layer. The via formed in the organo silicate glass layer is filled with an HSQ-based filler. The method further includes processing the surface of the HSQ-based filler filling the via formed in the organo silicate glass layer using plasma.

In the present invention of claims 39-52, a method of fabricating dual damascene interconnections includes forming a lower interconnection on a substrate and forming an etch stop on the lower interconnection. The method further includes forming an organo silicate glass layer on the etch stop layer and forming a via through the organo silicate glass layer to expose the etch stop. The via is filled with an HSQ-based filler. The surface of the HSQ-based layer filling the via formed through the organo silicate layer is processed using plasma.

It is stated in the Office Action, at page 3, lines 10-11, that Tsu, *et al.* fails to disclose processing the filler using plasma and the details about the plasma. Therefore, Tsu, *et al.* fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of a carbon-free inorganic filler filling a via formed in a dielectric layer using plasma, as claimed in claims 1-20. Tsu, *et al.* further fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of an HSQ-based filler filling a via formed in an organo silicate glass layer using plasma, as claimed in claims 21-38. Tsu, *et al.* further fails to teach or suggest a method of fabricating dual damascene interconnections that includes a surface of an HSQ-based layer filling a via formed through an organo silicate layer is processed using plasma, as claimed in claims 39-52.

Aoi discloses a resist pattern 12 formed having an opening over a region of an organic-inorganic hybrid film 11 to be used as a mask to form a wire groove or contact hole in the organic-inorganic hybrid film 11.

Aoi fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of a carbon-free inorganic filler filling a via formed in a dielectric layer using plasma, as claimed in claims 1-20. Aoi further fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of an HSQ-based filler filling a via formed in an organo silicate glass layer using plasma, as claimed in claims 21-38. Aoi further fails to teach or suggest a method of fabricating dual damascene interconnections that includes a surface of an HSQ-based layer filling a via formed through an organo silicate layer is processed using plasma, as claimed in claims 39-52.

Lee, *et al.* is cited in the Office Action as disclosing plasma treating a low k dielectric layer to densify the layer preventing damage caused by subsequent process. In Lee, *et al.*, an implantation step is performed on a dielectric layer 310. The dielectric layer 310 is etched to form openings 316a and 316b. A barrier layer is formed that covers the surfaces of the dielectric layer 310 in the opening. The openings 316a and 316b are then filled with a conductive material, forming via 320c and conductive line 320b.

In the present invention (see specification as filed at page 5, lines 3-10 and page 8, lines 12-27), a via filler is formed of a carbon-free inorganic material so that it can be dry etched at the same rate as a interlayer dielectric (ILD) and wet etched at a much higher rate than the ILD. During an exposure process for forming a photoresist pattern to define a subsequent trench, basic materials, such as nitrogen and amine, included in the ILD, may diffuse into a photoresist layer. Thus, the via filler is formed of a material that can prevent diffusion of the basic material into the photoresist layer.

Lee, *et al.* fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of a carbon-free inorganic filler filling a via formed in a dielectric layer using plasma, as claimed in claims 1-20. Lee, *et al.* further fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of an HSQ-based filler filling a via formed in an organo silicate glass layer using plasma, as claimed in claims 21-38. Lee, *et al.* further fails to teach or suggest a method of fabricating dual damascene interconnections that includes a surface of an HSQ-based layer filling a via formed through an organo silicate layer is processed using plasma, as claimed in claims 39-52. Instead, in Lee, *et al.*, a dielectric layer is ion implanted with a plasma treatment and later etched and filled with a barrier layer and conductive material to form via 320c and conductive line 320b.

Tsu, *et al.*, Aoi and Lee, *et al.* all disclose a material in which a via is formed. Specifically, in Tsu, *et al.*, a via 112 is formed in a via level dielectric 106 and a trench level dielectric 108. In Aoi, a depressed portion 13 composed of a wire groove or contact hole is formed in an organic-inorganic hybrid film 11. In Lee, *et al.*, openings 316a and 316b are formed in the dielectric layer 310.

Lee, *et al.* discloses plasma treating the dielectric layer 310 in which the openings 316a and 316b are formed, not the material that fills the openings 316a and 316b, as the applicants claim. So, the combination of Lee, *et al.* with Tsu, *et al.* and Aoi results in plasma treating the material in which the via is formed, not the material inside the via, which is not the applicants'

claimed plasma treatment of via filler 160 inside the via 150. None of the references teaches or suggests that the material filling the via is plasma treated.

Tsu, *et al.*, Aoi and Lee, *et al.* fail to teach or suggest these elements of the invention set forth in claims 1-20, 21-28, and 39-52. Specifically, none of the references teaches or suggests a method of fabricating dual damascene interconnections that includes processing a surface of a carbon-free inorganic filler filling a via formed in a dielectric layer using plasma, as claimed in claims 1-20, a method of fabricating dual damascene interconnections that includes processing a surface of an HSQ-based filler filling a via formed in an organo silicate glass layer using plasma, as claimed in claims 21-38, or a method of fabricating dual damascene interconnections that includes a surface of an HSQ-based layer filling a via formed through an organo silicate layer is processed using plasma, as claimed in claims 39-52. Accordingly, there is no combination of the references which would provide such teaching or suggestion. None of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 1-20, 21-28, and 39-52. Therefore, it is believed that the claims 1-20, 21-28, and 39-52. are allowable over the cited references, and reconsideration of the rejections of claims 1-10, 13, 16, 18-28, 31, 34, 36-43, 45, 48, and 50-52 under 35 U.S.C. § 103(a) based on Tsu, *et al.*, Aoi and Lee, *et al.*, is respectfully requested.

Robinson, *et al.* is cited in the Office Action as disclosing the use of H₂-based plasma to remove photoresist. Robinson, *et al.* fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of a carbon-free inorganic filler filling a via formed in a dielectric layer using plasma, as claimed in claims 1-20. Robinson, *et al.* further fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of an HSQ-based filler filling a via formed in an organo silicate glass layer using plasma, as claimed in claims 21-38. Robinson, *et al.* further fails to teach or suggest a method of fabricating dual damascene interconnections that includes a surface of an HSQ-based layer filling a via formed through an organo silicate layer is processed using plasma, as claimed in claims 39-52.

Robinson, *et al.*, like Tsu, *et al.*, Aoi and Lee, *et al.*, fails to teach or suggest these elements of the invention set forth in claims 1-20, 21-28, and 39-52. Accordingly, there is no combination of the references which would provide such teaching or suggestion. None of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 1-20, 21-28, and 39-52. Therefore, it is believed that the claims 1-20, 21-28, and 39-52. are allowable over the cited references, and reconsideration of the rejections of claims 17, 35 and 49 under 35 U.S.C. § 103(a) based on Tsu, *et al.*, Aoi, Lee, *et al.*, and Robinson, *et al.*, is respectfully requested.

Lui is cited in the Office Action as disclosing the use of an organic anti-reflective layer 85. Lui fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of a carbon-free inorganic filler filling a via formed in a dielectric layer using plasma, as claimed in claims 1-20. Lui further fails to teach or suggest a method of fabricating dual damascene interconnections that includes processing a surface of an HSQ-based filler filling a via formed in an organo silicate glass layer using plasma, as claimed in claims 21-38. Lui further fails to teach or suggest a method of fabricating dual damascene interconnections that includes a surface of an HSQ-based layer filling a via formed through an organo silicate layer is processed using plasma, as claimed in claims 39-52.

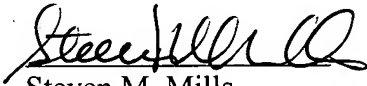
Lui, like Tsu, *et al.*, Aoi and Lee, *et al.*, fails to teach or suggest these elements of the invention set forth in claims 1-20, 21-28, and 39-52. Accordingly, there is no combination of the references which would provide such teaching or suggestion. None of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 1-20, 21-28, and 39-52. Therefore, it is believed that the claims 1-20, 21-28, and 39-52. are allowable over the cited references, and reconsideration of the rejections of claims 11-12, 14-15, 29-30, 32-33, 44 and 46-47 under 35 U.S.C. § 103(a) based on Tsu, *et al.*, Aoi, Lee, *et al.*, and Lui, is respectfully requested.

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Reply to Office Action of November 15, 2005

In view of the amendments to the claims and the foregoing remarks, it is believed that, upon entry of this Amendment, all claims pending in the application will be in condition for allowance. Therefore, it is requested that this Amendment be entered and that the case be allowed and passed to issue. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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